Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island

User Guide

March 2025
Revision 1.0

Important Notice:

1. **The content of this document is still under development and the product has yet to be verified. The information provided here is subject to change/modification in the next release.**

2. **The final version of the document will be available after the product has been validated.**

3 **Note that Arrow Island was designed to optimize thermal performance, it was not designed to account for solder joint reliability. Customers need to evaluate their system designs including the possible need for Board Level Underfill (BLUF) on the ARL processor to ensure solder joint reliability.**

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Contents

Figures

Tables

Revision History

Date	Revision	Description
January 2025	0.7	Initial release.
March 2025	1.0	Official release.

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1.0 Introduction

The Intel® Core™ Ultra Series 2 Processor Evaluation Kit based on the Intel® Edge Scalable Design Form Factor Reference Design is a powerful and efficient Internet-of-Things (IoT) development platform targeted for general embedded applications.

Intel® Edge Scalable Design uses a Mini-ITX 3.5" form factor (6.69" × 6.69"). It is a full performance computing platform in the smallest form factor possible which supports Arrow Lake - H – an Intel® Core™ Ultra hybrid processor built on a 7nm process with a TDP support of up to 45W.

To ensure optimal performance and reliability in diverse IoT environments, this evaluation kit utilizes key components from Innodisk Corp.:

- **Innodisk Industrial-grade SSD (4TG2-P Series):** Chosen for its exceptional endurance, reliability, and performance, this SSD enables rapid boot times, fast application loading, and robust data integrity – essential for demanding IoT applications.
- **Innodisk High-performance DDR5 6400 CSODIMM DRAM:** Renowned for their reliability and stability, Innodisk's high-performance DRAM modules are engineered to withstand wide temperature ranges and challenging operating conditions. This ensures consistent performance and longevity in demanding IoT deployments.
- **Innodisk MIPI Over Type-C Camera Kit:** This innovative kit overcomes the transmission limitations of standard MIPI-CSI cables (typically 20-30cm), extending the transmission distance to over 1 meter. This makes it ideal for applications requiring high-definition, real-time video transmission, such as AGVs, AMRs, and other scenarios where the camera needs to be positioned farther away.

For more detailed information about Innodisk products, please visit:
https://www.innodisk.com/cht/blog/intel-core-ultra-series2-reference-kit

This evaluation kit provides you with the necessary knowledge and understanding on the platform to enable you to customize the board design depending on your requirements. Alternatively, for faster time to market, this board design can be used as-is out of the box.

This user guide describes the typical hardware setup procedures, features and use of the Arrow Island Edge Scalable Design platform.

Note: It is important to read this document in its entirety before powering on the board.

Note: All diagrams displayed in this document are for illustration purposes only. The board you received may look different from the one shown in this document.

Note: 1. This evaluation kit is for research and development purposes only.

2. Electromagnetic interference and safety pre-certification test results for the evaluation kit are not ready upon current release. Intel may provide a revised user guide for the evaluation kit with the updated pre-certification test results.

1.1 Terminology

Table 1. Terminology

Term	Description
BIOS	Basic Input Output System
CMOS	Refers to the non-volatile configuration memory in the PCH
CPU	Central Processing Unit
DDR5	Double Data Rate 5 Synchronous Dynamic Random-Access Memory fifth generation
DP	DisplayPort
GND	Signal Ground
GPIO	General-Purpose Input Output
HDD	Hard disk drive
HDMI	High Definition Multimedia Interface
LAN	Local Area Network
LED	Light Emitting Diode
ME	Intel Management Engine
OS	Operating System
PCB	Printed Circuit Board
PCIe	Peripheral Component Interface Express
RTC	Real Time Clock
SATA	Serial – Advanced Technology Attachment
SBC	Single Board Computer
SIO	Super Input Output
SLP	Sleep
SO-DIMM	Small Outline Dual In-line Memory Module

Term	Description
SSD	Solid State Drive
SPI	Serial Peripheral Interface
eSPI	Embedded Serial Peripheral Interface
SVID	Serial Voltage Identification
TDP	Thermal Design Power
TPM	Trusted Platform Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UFS	Universal Flash Storage

1.2 Evaluation Kit System Supported OS

The evaluation kit system contains the item listed in Table 2 and supports the following OS listed in Table 3 based on the BIOS version.

Table 2. Evaluation Board System

Evaluation Board Parts	Model Number
Arrow Island Fab B	N47228-200

Table 3. List of OS Supported by the Evaluation Kit System

BIOS Version	Supported OS
Arrow Island PV BIOS	Windows 10
	Windows 11
	Ubuntu

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2.0 Getting Started

Before using the evaluation kit, verify that all the items listed in this section are received, and that the evaluation board is functioning by going through the following:

- Check the contents of the evaluation kit.
- Inspect the evaluation board for any defects.
- Power-on the evaluation board and verify that it is functioning correctly.

2.1 Before You Begin

Verify the contents of the evaluation kit and the condition of the evaluation board. If any of the items are missing or if the evaluation board is damaged, contact Intel before you proceed.

Note: Make sure the RTC battery is connected onboard. Without RTC battery, the board will not be able to power up smoothly.

2.1.1 Check the Contents of the Evaluation Kit

The Intel® Core™ Ultra Processor Reference Design based on Intel® Edge Scalable Design contains the following items:

- Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design System
- 12V@15A DC Power Adapter
- Safety Flyer
- China RoHS Table (MDDS)
- Intel® Development Vehicles Terms and Condition

2.1.2 Inspect the Evaluation Board

To check the evaluation board for damages, set it on an anti-static surface and inspect the evaluation board to ensure that the components are not missing, bent, or cracked.

Warning: The evaluation board may be damaged if it is not placed on an anti-static surface.

2.1.3 Power-on the Evaluation Board

Once the evaluation board is free from any visible defects, power-on the evaluation board and verify that the evaluation board is functioning correctly using the following steps:

1. Connect the supplied DC power adapter to the evaluation board (only use the DC power adapter supplied with the evaluation kit).
2. Hit the **ESC** key as the system boots to enter the BIOS setup screen.
3. Check the time, date, and configuration settings. The default settings should be sufficient for most users except for Intel® SpeedStep® Technology. This feature is disabled by default and can be enabled in setup.
4. Save and exit the BIOS setup.
5. The system will reboot and would then be ready for use.

Note: The evaluation board can be powered down with the following methods:

- Use the Windows Start menu (or equivalent) shutdown option.
- If the above does not work, hold down the power button for 7 seconds to asynchronously shut down the system (not recommended).

2.2 Reference Documents

Log in to the Resource and Design Center (rdc.intel.com) to search for and download the document numbers listed in the following table. Contact your Intel field representative for access.

Note: Third-party links are provided as a reference only. Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

Table 4. Reference Documents

Document	Document No./Location
Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island - Schematics PDF	822991
Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island - Schematics Cadence Format	822992
Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island - Bill of Materials (BOM)	822997
Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island - Tape Out Manufacturing Files	822998
Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island - Schematics Cadence Format	822992

Document	Document No./Location
Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island - Schematics OrCAD Format	822993
Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island - Schematics Zuken Format	822994
Intel® Core™ Ultra Series 2 Processor Reference Design based on Intel® Edge Scalable Design – Arrow Island - Schematics Mentor Format	822995
Arrow Lake-UH Platform Design Guide	772237
Intel® Core™ Ultra Series 2 Processor External Design Specification (EDS), Volume 1 of 2	777369

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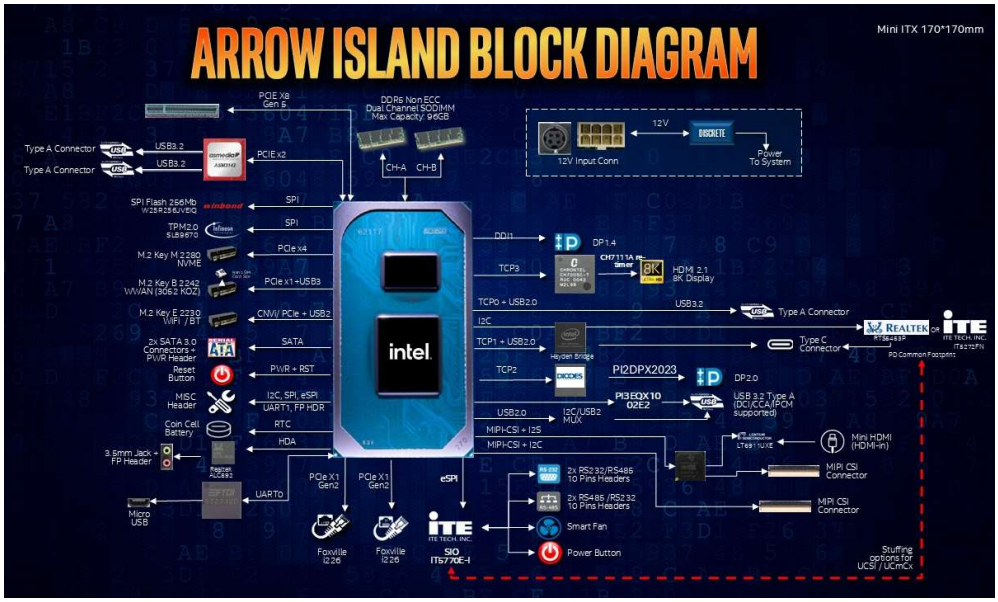
3.0 Evaluation Kit Overview

3.1 Block Diagram

Figure 1. Block Diagram of the Evaluation Kit



3.2 Features and Specifications

Table 5. Features and Specifications Table

Features	Specifications	Details
CPU	Family Package type TDP Package Size	Intel® Core™ Ultra Processor Series 2 BGA 2049 45W 25.0x50.0mm
Memory	RAM type Maximum RAM capacity Maximum RAM speed RAM slot	DDR5 (5.0V) 96GB 6400MT/s 2 x SODIMM
BIOS	SPI model	W25R256JWEIQ 256M-bit WSON-8 NOR flash memory 1 x 16pin SPI header
Display Out	Onboard display ports Display interfaces[1] Integrated audio Maximum resolution	1 x HDMI, 2 x DP, 1 x USB Type-C TCP – DisplayPort* Alt Mode on USB Type-C – USB A – HDMI 2.1 – DP 2.0 Integrated Supported 7680x4320 60Hz
Display In	CSI	1 x Micro HDMI-in port (CSI to HDMI converter LT6911UXE U2)
Storage	PCIE slots Standard HDD/SSD SATA	1 x M.2 Key M 2280 slot (NVMe PCIE Gen4) 2 x SATA Connector, 2 x SATA power header
USB	USB 3.2 Gen 2 USB 3.2 Gen 1	1 x USB 3.2 Gen 2 Type-C ports 4 x USB 3.2 Gen 1 Type-A ports
Network	Gigabit LAN port Ethernet Controller WiFi/BT WWAN (LTE/5G)	2 x RJ45 port 2.5Gbps 2 x Foxville I226-IT (Ethernet Port 1&2) 1 x M.2 Key E 2230 slot (PCIe/USB2.0) 1 x M.2 Key B 3052 slot (PCIe/USB3.0)
Serial Port	COM port header	2 x RS232 header 2 x RS485 header
SIO	eSPI/LPC 2 UARTs Super I/O	ITE IT5770E-I
Power Supply	DC Power Adapter Power Connector	12V @15A input DC power adapter (GST220A12-R7B 220W) 1 x 4pin mini-DIN[2] 1 x 8pin CPU ATX Power Connector[2] (optional)

Features	Specifications	Details
Others	RTC SPI TPM Fan header UART header eSPI header Front panel header	1 x RTC header 1 x TPM2.0 SLB9670VQ2.0 2 x Fan power header (1 Smart Fan) 1 x 4pin header 1 x 10pin header 1 x 10pin header
PCB	Board Form Factor Z-height (incl. components) PCB thickness PCB layer count PCB type	6.69" x 6.69"/169.9mm x 169.9mm 1.0"/25.12mm 1.6mm 10 layers Type 3

NOTES:

1. Maximum four displays at one time.
2. Plug in only 1 power source at a time. Default power connector is 4 pin mini-DIN.

3.3 System Power Management States

Table 6 lists the power management states that have been defined for the platform. The Controller Link (CL) operates at various power levels called M-states.

Table 6. Arrow Lake Advanced Configuration and Power Interface (ACPI)

State	Power Well Description
G0 / S0 / C0	**Full On:** CPU operating. Individual devices may be shut to save power. The different CPU operating levels are defined by Cx states.
G0 / S0/ Cx	**Cx state:** CPU manages C-states by itself and can be in low power state.
G1	**Suspend-To-RAM (STR):** The system context is maintained in system DRAM, but power is shut to non-critical circuits. Memory is retained, and refreshes continue. All external clocks are shut off; RTC clock and internal ring oscillator clocks are still toggling. In SLP_S3 signal stays asserted, SLP_S4 and SLP_S5 are inactive until a wake occurs.
G1 / S4	**Suspend-To-Disk (STD):** The context of the system is maintained on the disk. All power is then shut to the system except to the logic required to resume. Externally appears same as S5 but may have different wake events. In S4, SLP_S3 and SLP_S4 both stays asserted and SLP_S5 is inactive until a wake occurs.
G2 / S5	**Soft Off:** System context not maintained. All power is shut except for the logic required to restart. A full boot is required when waking. Here, SLP_S3, SLP_S4, and SLP_S5 are all active until a wake occurs.

State	Power Well Description
G3	**Mechanical OFF:** System context not maintained. All power shut except for the RTC. No "Wake" events are possible because the system does not have any power. This state occurs if the user removes the batteries, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns the transition will depend on the state just prior to the entry to G3.

Table 7 lists the power management states that have been defined for the platform.

Table 7. Arrow Lake Power Rail Descriptions

Power Type	Voltage Range (V)	Power Well Description
VCCPRIM_1P8	1.8	1.8 V Primary Well.
VCCPRIM_3P3	3.3	3.3 V Primary Well.
VCCPRIM_IO	1.25	1.25 V Primary Well.
VCCPRIM_VNNAON	0.77	0.77 V Primary Well.
VCCPRIM_VNNAON_FLTRA	0.77	VNNAON with filter requirements
VCCPRIM_VNNAON_FLTRB	0.77	VNNAON with filter requirements
VCCPRIM_1P8_FLTRA	1.8	V1P8_A with filter requirements
VCCPRIM_1P8_FLTRB	1.8	V1P8_A with filter requirements
VCCCORE	0 ~ 1.52	Dynamic SVID power rail for IA cores
VCCGT	0 ~ 1.52	Dynamic SVID power rail for graphics
VCCSA	0 ~ 1.52	Dynamic SVID power rail for system agent
VDD2	1.1	Fixed 1.05/1.10 V power rail for memory host controller
VCCRTC	1.5	RTC Well Supply. This power is not expected to be shut off unless the RTC battery is removed or drained. **NOTES:** 1. VCCRTC nominal voltage is 1.5 V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. 2. Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VSS	-	Ground

The voltage of the evaluation board power nets at different activity states is shown in Table 8.

Table 8. Platform Voltage Regulator Power Rail

Power Net	Voltage (V)	Power Well
V12_ADP	12.0	POWER SOURCE
V12_A	12.0	ALWAYS ON
V5_A	5.0	ALWAYS ON
V3P3_A	3.3	ALWAYS ON
V1P8_A	1.8	ALWAYS ON
V2P5_A	2.5	ALWAYS ON
V1P1_A	1.1	ALWAYS ON
V3P3A_RTC	3.3	CORE
VNNAON	0.77	CORE
VCCIO	1.25	CORE
VDD2	1.1	CORE
VCCIA	0 ~ 1.52	CORE
VCCGT	0 ~ 1.52	CORE
VCCSA	0 ~ 1.52	CORE
V12_S	12.0	PLATFORM
V5_S	5.0	PLATFORM
V3P3_S	3.3	PLATFORM
V1P8_S	1.8	PLATFORM
V1P2_S	1.2	PLATFORM
V1P1_S	1.1	PLATFORM
V1P8_A_SPI_CON	1.8	PLATFORM
V1P8_A_LVDS	1.8	PLATFORM
VDD_LVDS	3.3	PLATFORM
V5A_USB_CONN1	5.0	PLATFORM
V5A_USB_CONN2	5.0	PLATFORM
V3P3_A_LAN	3.3	PLATFORM
V5_TYPEC_VT	5.0	PLATFORM
V5_TYPEC_RA	5.0	PLATFORM

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4.0 Evaluation Kit Setup

This section provides the following details:

- Lists the major components and their locations on the evaluation board, front panel, and back panel.
- Describes the pinouts of the headers.
- Lists the LED indicator location and colors for different power states.
- Provides the configuration settings to clear the BIOS.

4.1 List of Component

The following figures and tables show the evaluation board (top and bottom), including the location of each major components with the reference designators.

Figure 2. Board Top Layer

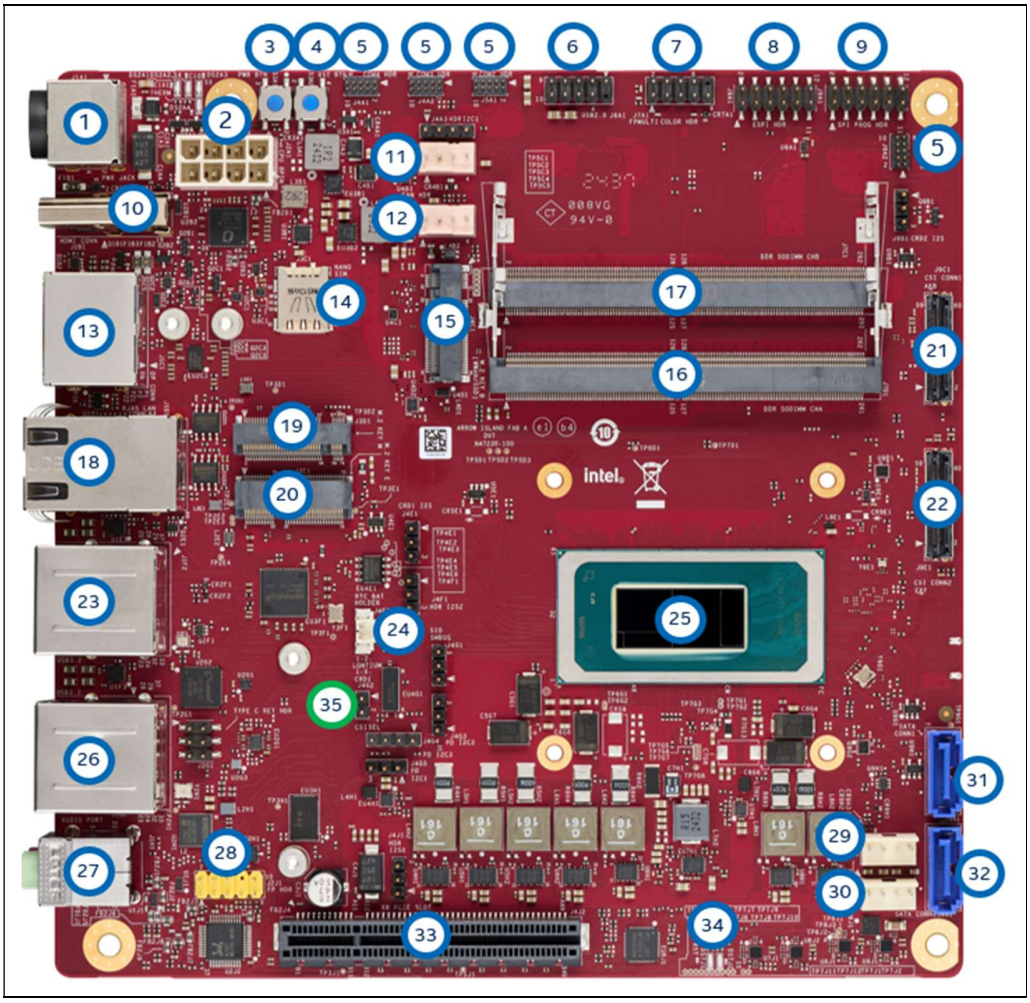

Table 9. Board Top Layer Description

Item Number	Description	Reference Designator
1	4 pin mini-DIN Power Jack	J1A1
2	8-pin CPU ATX power connector	J2A1
3	Power button	S3A1
4	Reset button	S3A2
5	COM port header (RS232 + RS485)	J9A2, J5A1, J4A2, J4A1
6	USB2 front panel header	J6A1
7	Front panel header	J7A1
8	ESPI header	J8A1
9	DediProg SF600 Programming SPI Header	J9A1

Item Number	Description	Reference Designator
10	HDMI connector	J1B1
11	Full speed fan header	J4A4
12	Smart fan header	J4B1
13	DP stack connector	J1C1
14	Nano SIM card tray	J3C1
15	M.2 Key B connector	J4C1
16	DDR5 SODIMM Connector CH-A	J7D1
17	DDR5 SODIMM Connector CH-B	J7C1
18	RJ45 stack connector	J1D1
19	M.2 Key M connector	J3D1
20	M.2 Key E connector	J3E1
21	MIPI CSI connector 1	J9C1
22	MIPI CSI connector 2	J9E1
23	High rise USB A stack connector	J1F2
24	RTC battery header	J4F2
25	Intel® Core™ Ultra Processor	U7F1
26	High rise USB A stack connector	J1G2
27	3.5mm Audio connector (Audio out + Mic in)	J1H1
28	Intel HD Audio front panel	J2J1
29	SATA power header	J9H2
30	SATA power header	J9J2
31	SATA connector 1	J9H1
32	SATA connector 2	J9J1
33	PCIe Gen5 x8 slot	J4J2
34	LED	DS7J1, DS7J2
35	CSI selection header (Multiplexer)	J4G2

Figure 3. Board Bottom Layer

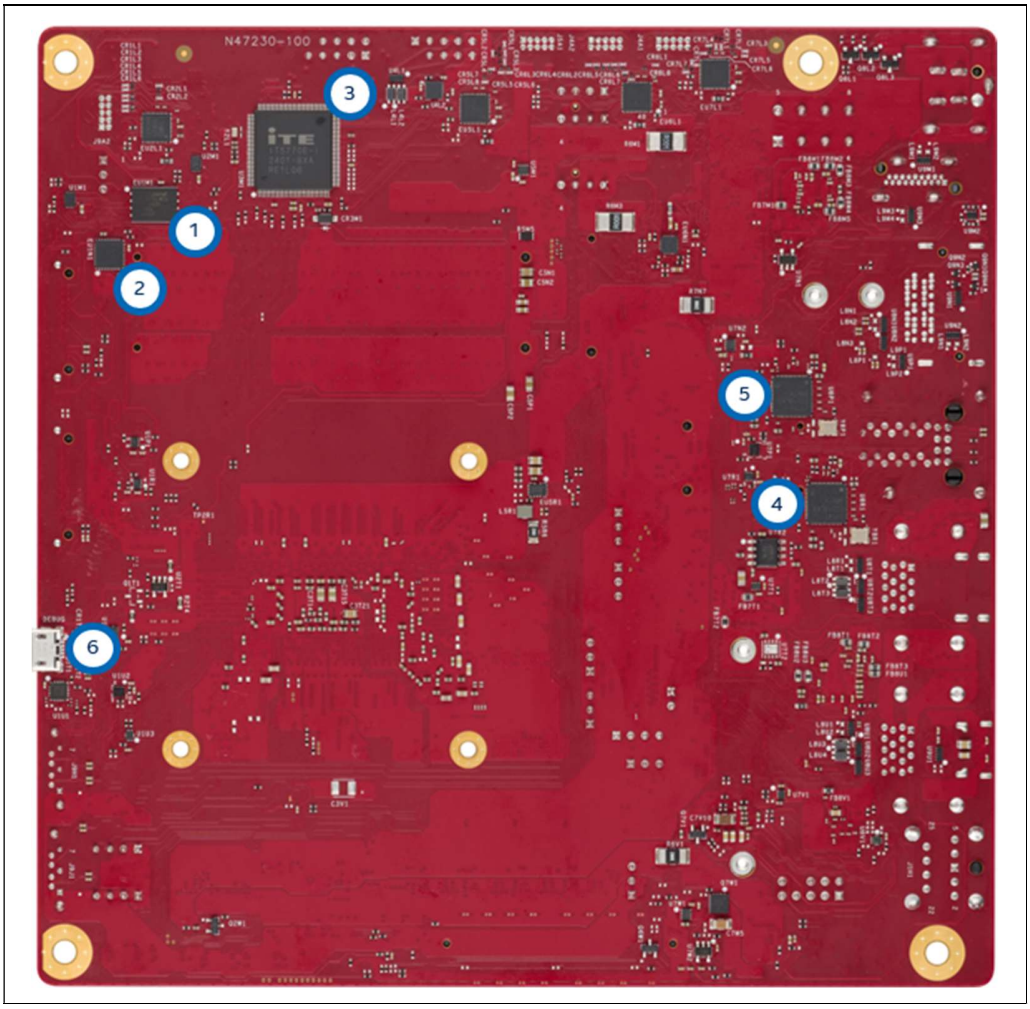

Table 10. Board Bottom Description

Item Number	Description	Reference Designator
1	BIOS SPI W25R256JWEIQ	EU1M1
2	SPI TPM2.0 SLB9670VQ2.0	EU1N1
3	Super I/O ITE IT5770E-I	U3M1
4	LAN Controller Foxville I226 (Lan 1)	U8R2
5	LAN Controller Foxville I226 (Lan 2)	U8P2
6	Micro USB Debug connector	J1T1

Figure 4. Board Back Panel

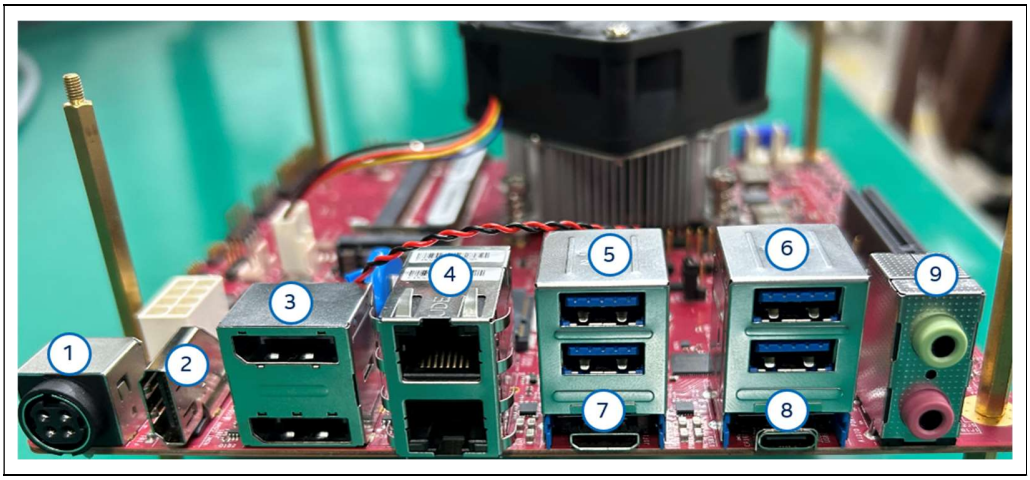

Table 11. Board Back Panel Description

Item Number	Description	Reference Designator
1	4 pin mini-DIN	J1A1
2	HDMI connector	J1B1
3	DP stack connector	J1C1
4	RJ45 stack connector	J1D1
5	High rise USB A stack connector	J1F2
6	High rise USB A stack connector	J1G2
7	Mini HDMI connector (HDMI IN)	J1F1
8	USB Type-C right angle connector	J1G1
9	3.5mm Audio connector (Audio out + Mic in)	J1H1

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4.2 Header Pinout Configuration

4.2.1 Evaluation Board Header Pinout

The following tables list the pinout configuration for the headers, and their corresponding signal names, on the evaluation board.

Table 12. Serial COM RS232 Port 1/4 Header (J9A2/J4A1), RS485 Port 2/3 Header (J5A1/J4A2)

Pin	Signal Name	Pin	Signal Name
1	HDR1/2/3/4_DCD_N	2	HDR1/2/3/4_RX
3	HDR1/2/3/4_TX	4	HDR1/2/3/4_DTR_N
5	GND	6	HDR1/2/3/4_DSR_N
7	HDR1/2/3/4_RTS_N	8	HDR1/2/3/4_CTS_N
9	HDR1/2/3/4_RI_N	10	NC

Table 13. Intel HD Audio Front Panel (J2J1)

Pin	Signal Name	Pin	Signal Name
1	HDR_MIC2_L	2	AGND_HDA
3	HDR_MIC2_R	4	HDR_AUD_DET_N
5	HDR_FRONT2_R	6	HDR_FP_MIC_SEN
7	HDA_JD3_R	8	NC
9	HDR_FRONT2_L	10	HDR_FP_AUD_SEN

Table 14. USB2 Front Panel Header (J6A1)

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	GND	4	GND
5	USB2_P9_C_DP	6	USB2_P7_C_DP
7	USB2_P7_C_DN	8	USB2_P7_C_DN
9	V5_USB2_FP2	10	V5_USB2_FP1

Table 15. Front Panel Header (J7A1)

Pin	Signal Name	Pin	Signal Name
1	SATA_LED_PWR (3.3V)	2	FRONT_LED (3.3V)
3	SATA_LED_N	4	GND
5	GND	6	FP_PWRBTN_N
7	FP_SYSRST_BTN_N	8	GND
9	V3P3_s	10	NC

Table 16. ESPI Header (J8A1)

Pin	Signal Name	Pin	Signal Name
1	V1P8_A / V3P3_A	2	GND
3	HDR_ESPI _CLK	4	HDR_ESPI _IO_3
5	HDR_ESPI_CS1_N	6	HDR_ESPI _IO_2
7	HDR_ESPI_CS0_N	8	HDR_ESPI _IO_1
9	HDR_ESPI_RESET_N	10	HDR_ESPI _IO_0
11	HDR_ESPI_ALERT0_N	12	V3P3_S

Table 17. RTC Battery Header (J4F2)

Pin	Signal Name
1	HDR_RTC_BATT
2	GND

Table 18. I2C1 Header (J4A3)

Pin	Signal Name
1	V3P3_S
2	I2C1_SCL
3	I2C1_SDA
4	GND

Table 19. SATA Power Header (J9H2/J9J2)

Pin	Signal Name
1	V12_S
2	GND
3	GND
4	V5_S

Table 20. Full Speed Fan Header (J4A4)

Pin	Signal Name
1	GND
2	V12_S
3	NC
4	HDR_FAN_2_CTL (V5_S)

Table 21. Smart Fan Header (J4B1)

Pin	Signal Name
1	GND
2	V12_S
3	HDR_FANIN_R
4	HDR_FAN_1_CTL

Table 22. Dediprog SF600 Programming SPI Header (J9A1)

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	SPI0_CS0_R_N	4	V1P8_A_SPI_CON
5	SPI0_MISO_HDR	6	SPI0_HOLD_N_HDR
7	SPI0_DQ2_HDR	8	SPI0_CLK_HDR
9	GND	10	SPI0_MOSI_HDR
11	NC	12	DEDIPROG_RST

Table 23. MIPI CSI connector (J9C1)

Pin	Signal Name	Pin	Signal Name
1	NC	2	V5_S
3	GND	4	NC
5	V12_S	6	NC
7	V12_S	8	CRD1_A0
9	IMG_CLK_OUT_R_3	10	CRD1_A1
11	GND	12	NC
13	IMG_CLK_OUT_R_2	14	GND
15	CRD1_PRIVACY_LED	16	I2S_WS (HDR)
17	CRD1_CLK_EN	18	NC
19	GPP_V23_CRD_RST_R_N	20	I2S_D0 (HDR)
21	CRD1_PWR_EN	22	I2S_SCLK (HDR)
23	CRD1_CAM_STROBE	24	GND
25	CRD1_I2C0_SDA	26	CSI_B_CLK_DN
27	CRD1_I2C0_SCL	28	CSI_B_CLK_DP
29	CRD1_SYNC_IN	30	GND
31	CRD1_SYNC_OUT	32	CSI_B1_A3_DN
33	GND	34	CSI_B1_A3_DP
35	NC	36	GND
37	GND	38	CSI_B0_A2_DN
39	NC	40	CSI_B0_A2_DP
41	V1P8_S	42	GND
43	V1P8_S	44	CSI_A_CLK_DN
45	GND	46	CSI_A_CLK_DP
47	NC	48	GND
49	GND	50	CSI_A1_DN
51	GND	52	CSI_A1_DP
53	GND	54	GND
55	V3P3_S	56	CSI_A0_DN
57	V3P3_S	58	CSI_A0_DP
59	V3P3_S	60	GND

Note: This connector shares I2C0 with onboard Lontium. Please empty/unstuff the unused I2C pair to use Lontium AIC. Default CSI lanes are to Lontium IC. Please disconnect (1-x) J4G2 jumper to select this connector.

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Table 24. MIPI CSI connector 2 (J9E1)

Pin	Signal Name	Pin	Signal Name
1	NC	2	V5_S
3	GND	4	NC
5	V12_S	6	NC
7	V12_S	8	CRD2_A0
9	IMG_CLK_OUT_R_1	10	CRD2_A1
11	GND	12	NC
13	IMG_CLK_OUT_R_0	14	GND
15	CRD2_PRIVACY_LED	16	I2S_WS
17	CRD2_CLK_EN	18	NC
19	GPP_H00_CRD_RST_R_N	20	I2S_D0
21	CRD2_PWR_EN	22	I2S_SCLK
23	CRD2_CAM_STROBE	24	GND
25	CRD2_I2C3_SDA	26	CSI_F_CLK_DN
27	CRD2_I2C3_SCL	28	CSI_F_CLK_DP
29	CRD2_SYNC_IN	30	GND
31	CRD2_SYNC_OUT	32	CSI_F1_E3_DN
33	GND	34	CSI_F1_E3_DP
35	NC	36	GND
37	GND	38	CSI_F0_E2_DN
39	NC	40	CSI_F0_E2_DP
41	V1P8_S	42	GND
43	V1P8_S	44	CSI_E_CLK_DN
45	GND	46	CSI_E_CLK_DP
47	NC	48	GND
49	GND	50	CSI_E1_DN
51	GND	52	CSI_E1_DP
53	GND	54	GND
55	V3P3_S	56	CSI_E0_DN
57	V3P3_S	58	CSI_E0_DP
59	V3P3_S	60	GND

4.3 Push-Buttons and LED Indicators

4.3.1 Power-On Button

The Power button enables or disables power to the entire evaluation kit system causing it to boot or shut down. The location of the Power button is shown in Table 25.

Table 25. Push-Buttons Location Table

Description	Reference Designator
Power Button	S3A1
Reset Button	S3A2

4.3.2 Power Button LED Indicator

The location, power state, and color of the Power button LED indicator are shown in Table 26.

Table 26. LED Indicators Table

Description	Reference Designator	Power State	Color
3.3V A-rail	DS7J2	S5	Green
Platform Reset	DS7J1	S0	Green
S5	DS2A3	S5	Green
S4	DS2A1	S4	Green
Thermtrip	DS2A4	N/A	Red

4.4 Configuration Settings

4.4.1 J4F2 — Clear/Keep CMOS Settings

Clearing the contents of all CMOS and BIOS settings will restore the evaluation kit system to factory default values.

Note: J4F2 is connected to a coin cell battery by default.

Follow the steps to restore the BIOS settings:

1. Turn off the evaluation kit system and unplug the power cord.
2. Unplug the coin cell battery at J4F2 for 10s
3. Plug in the coil cell battery at J4F2.
4. Turn on the evaluation kit system.

5.0 BIOS Setting

5.1 Flashing BIOS with DediProg SF600

The DediProg* SF600 programmer can be used to program the SPI flash device for Arrow Island to boot from SPI flash.

The steps are as follows:

1. Install the latest DediProg software from the DediProg website (http://www.dediprog.com) onto your host system.
2. The SPI flash can be programmed in Single I/O mode as well as Quad mode for higher speed.
3. Connect the USB cable of the DediProg programmer to the system on which you have installed the software.
4. Connect the ISP Cable (**ISP-600-CB1-G**) to the SPI DediProg header at J9A1.
5. No jumper settings needed.
6. Launch the DediProg tool and confirm the settings from Config → Miscellaneous Settings → Quad IO option → Enable Quad IO (for Quad mode). Default is Single I/O.
7. Set the Vcc option to 1.8V prior to auto detect. The programmer's pin header output is 1.8V.
8. Ensure that "Currently Working On" is in "Application Memory Chip 1".
9. Go to "File" and select the *.bin* file to program Chip1.
10. Execute the batch operation to erase and flash the *.bin* image corresponding to SPI and verify the image.
11. Close DediProg software manually, it will store the settings.
12. Remove the DediProg SF600 programmer.

Note: Be sure to unplug the DediProg SF600 programmer before powering up the Arrow Island board. With the programmer plugged onboard while powering up the board may cause failure to boot.

5.2 Feature Enabling Setting

Refer to Feature Enabling BKM and Hardware guide

5.3 Important Notes

Please read the information below carefully for these respective features:

1. **MIPI CSI**

   A part of the MIPI CSI lanes are being multiplexed for optional header support. Please make sure J4G2 selection is correct:

   1-2 = Onboard Lontium (U2G2 and J1F1)

   1-x = CSI Conn 1 (J9C1)

   For using Lontium AIC on J9C1, please unstuff R8U1 and R8U2 resistors to avoid I2C address clash with onboard Lontium.

2. **Serial COM Ports**

   Due to hardware limitations, COM3 (J4A2) can only be used as RS485.

3. **UCSI Feature**

   For customers following Arrow Island's Type-C design for single Type-C port, please use Port A instead of Port B as the default port.